IN THE CLAIMS:

1. (Twice Amended) A data processing arrangement comprising:

a first processor for providing successive sets of input data;

a second processor for receiving successive sets of output data;

a memory system comprising a plurality of independent memory circuits accessible by the first processor and the second processor for receiving the successive sets of input data and providing the successive sets of output data;

B1

a master controller for setting up the plurality of independent memory circuits of said memory system using control commands associated with a set of input data and a set of output data; and

a control unit for, on the basis of the control commands, selecting a first memory circuit and generating a write-address for the first memory circuit when a data from the set of input data provided by the first processor, and for, on the basis of the control commands, selecting a second memory circuit and generating a read-address for the

B1 end

second memory circuit when a data from the set of output data is required by the second processor.

4. (Twice Amended) A memory system comprising:

a plurality of independent memory circuits for receiving successive sets of input data and for providing successive sets of output data;

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a control unit being programmable by means of control commands associated with a set of input data and a set of output data and, on the basis of these control commands, for selecting a first memory circuit and generating a write-address for the first memory circuit, when a data from the set of input data is received, and for selecting a second memory circuit and generating a read-address for the second memory circuit, when a data from the set of output data is provided.

5. (Twice Amended) A method of processing data in a data processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of independent memory circuits shared by both the first processor and the second